REMARKS

Claims 1-5, 12-22 and 29-34 are rejected. Claims 6-11 and 23-28 are objected to. Claims 5, 7, 10, 11, 13, 22, 24, 27, 28, and 30 are currently amended. Claims 35-44 are newly added. Claims 1-44 are currently pending.

Claim Objections

Claim 31 was objected to because line 1 of claim should have referenced claim 18 instead to claim 26. Applicants amend claim 31 to reference claim 18, and respectfully request withdrawal of the objection to claim 31.

Claim Rejections - 35 USC § 102

Claims 1-5, 14-22 and 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Lockyear (U.S. Patent No. 6,336,206).

Lockyear states "[a post-synthesis] gate-level netlist may then undergo several succeeding transformations.... After each of these succeeding transformations, formal verification can be used to verify that the result of the latest transformation is functionally equivalent to the resulting gate-level netlist of the preceding transformation." (Lockyear, column 1, lines 39-48)

In Lockyear, at each transformation step, a single preceding netlist exists. The single preceding netlist is transformed to produce a succeeding netlist. The succeeding netlist exists only after the succeeding netlist has been created by transformation of the preceding netlist. In Lockyear, because the succeeding netlist does not even exist until the preceding netlist undergoes a transformation, information about the succeeding netlist cannot be used to guide the transformation of the preceding netlist.

In contrast with Lockyear, claim 1 claims in part: "resynthesizing the first gate-level representation of the circuit design to incorporate the learned architecture information from the second gate-level representation of the circuit design".

Again in contrast with Lockyear, claim 18 claims in part: "resynthesize the first gate-level representation of the circuit design to incorporate the learned architecture information from the second gate-level representation of the circuit design".

An example of a first gate-level representation is shown in Figure 1 of the patent application as "Gate Level Representation of Golden Circuit 106". An example of a second gate-level

representation is shown in Figure 1 of the patent application as "Gate Level Representation of Revised Circuit Generated by Synthesis Tool 104".

Because Lockyear teaches that only a single netlist is input for each transformation, Lockyear fails to teach claims 1 (and dependent claims 2-5 and 14-17) and 18 (and dependent claims 19-22 and 31-34). Withdrawal is respectfully requested of the 35 U.S.C. 102(e) rejection to claims 1-5, 14-22 and 31-34.

Claim Rejections - 35 USC § 103

Claims 12, 13, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lockyear in view of Sharma et al. (U.S. Patent No. 5,841,663).

Lockyear teaches that, for each transformation of a gate-level netlist, only a single netlist is input.

Sharma teaches the transformation of a register transfer-level circuit description, typically in a hardware description language such as Verilog or VHDL, into a gate-level circuit netlist.

In contrast with Lockyear and Sharma, claim 1 claims in part: "resynthesizing the first gate-level representation of the circuit design to incorporate the learned architecture information from the second gate-level representation of the circuit design"

Again in contrast with Lockyear and Sharma, claim 18 claims in part: "resynthesize the first gate-level representation of the circuit design to incorporate the learned architecture information from the second gate-level representation of the circuit design"

Lockyear and Sharma, alone and in combination, fail to teach or suggest claim 1 (and dependent claims 12 and 13) and claim 18 (and dependent claims 29 and 30). Withdrawal is respectfully requested of the 35 U.S.C. 103 rejection to claims 12, 13, 29, and 30.

CONCLUSION

It is submitted that the present application is in form for allowance, and such action is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required, including petition fees and extension of time fees, to Deposit Account No. 23-2415 (Docket No. 19329-714). A duplicate copy of this paper is enclosed.

Respectfully submitted,

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